DYNAMIC CONTROL OF SWITCHING REFERENCEVOLTAGE

FIELD OF THE INVENTION

[0001] This invention relates generally to electronic circuits and more particularly to methods and circuits for receiving digital electronic signals.

BACKGROUND OF THE INVENTION

[0002] Digital electronic signals are used to communicate digital information. This communication may be from on device to another, one integrated circuit (or chip) to another, or within an integrated circuit itself. In many of these applications, the difference between the a voltage level that denotes a "high" (or logical "1") and the voltage level that denotes a "low" (or logical "0") has been getting smaller. Designers have chosen these smaller differentials for reasons that include: lower power supply voltages, increasing switching speed, lowering power consumption, and the use of standard bus interfaces that have defined smaller voltage differentials.

[0003] Unfortunately, these smaller voltage differentials are harder to detect, especially in the presence of noise or other non-idealities on the signal. Accordingly, there is a need in the art for improvements that help with the detection and reception of digital signals having small voltage differentials between logical levels.

SUMMARY OF THE INVENTION

[0004] A reference voltage is moved dynamically towards a voltage level of the last received value. The movement takes place over a predetermined fraction of a bit time. The amount of movement is limited so that successive logical values don't result in an unusable reference voltage level.

[0005] Other aspects and advantages of the present invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] FIG. 1 is voltage vs. time plot of an exemplary input signal, a dynamically controlled reference voltage, and a static reference voltage.

[0007] FIG. 2 is a flowchart illustrating steps to dynamically control a reference voltage.

[0008] FIG. 3 is a schematic diagram illustrating a circuit that dynamically controls a reference voltage.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0009] FIG. 1 is voltage vs. time plot of an exemplary input signal **102**, a dynamically controlled reference voltage **104**, and a static reference voltage **106**. In FIG. 1, note how the dynamically controlled reference voltage **104** moves toward the voltage level of the exemplary input signal **102** after each transition of the exemplary input signal **102**. The movement is shown taking place over a period of time that approximates one-half a bit-time, t_{bit}. A bit-time is the normal period of the maximum data frequency. Once the dynamically

controlled reference voltage **104** reaches a predetermined level, it stays approximately constant until another transition takes place on the input signal **102**.

[0010] V_A and V_B illustrate the minimum voltage differential between the input signal **102** and the dynamically controlled reference voltage **102** shortly after a transition. This minimum voltage differential may eventually become smaller as the dynamically controlled reference voltage **104** moves toward the input signal **102**, but by then, much of the noise on the input signal **102** has settled out so the input signal **102** doesn't cross the dynamically controlled reference voltage **104**. Note that V_A and V_B are both larger than the minimum voltage differential between the input signal **102** and the static reference voltage **106** at the same point in time. Accordingly, at this critical time shortly after an input signal **102** transition, the noise margin for the dynamically controlled reference signal **104** is larger than the noise margin for the static reference signal **106**.

[0011] Also note that, as shown in FIG. 1, it takes less time for the input signal **102** to cross the dynamically controlled reference voltage **104** than it does the static reference voltage **106**. This is shown as At in FIG. 1. Since the dynamically controlled reference voltage **104** has moved closer to the input signal **102** voltage than the static reference voltage **106** (which does not move) near the end of each bit-time, an input signal **102** transition with a non-infinite slope crosses the dynamically controlled reference voltage **104** level sooner than it crosses the static reference voltage **106** level. This illustrates that an input signal **102** transition can be detected faster with the dynamically controlled reference voltage **104** than it can be detected with a static reference voltage **106**.

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[0012] FIG. 2 is a flowchart illustrating steps to dynamically control a reference voltage. In a step **202**, an initialization decision is made. If the current state of the input signal is at a high low voltage, flow proceeds to step **214**. If the current state of the input signal is a low voltage, flow proceeds to step **204**. In a step **204**, the system waits for a transition. Since it was determined in step **202** that the current state of the input signal was at a low voltage, or because flow to step **204** came from step **216** just

after a high-to-low transition, the transition in step **204** would be a low-to-high transition. After this transition, flow proceeds to step **206**. In a step **206**, the reference voltage is ramped-up from its present voltage to a higher voltage. Flow then proceeds to step **214**.

[0013] In a step **214**, the system waits for a transition. Since it was determined in step **202** that the current state of the input signal was at a high voltage, or because low to step **214** came from step **206** just after a low-to-high transition, the transition in step **214** would be a high-to-low transition. After this transition, flow proceeds to step **216**. In a step **216**, the reference voltage is ramped-up from its present voltage to a higher voltage. Flow then proceeds to step **204**.

[0014] FIG. 3 is a schematic diagram illustrating a circuit that dynamically controls a reference voltage. In FIG. 3, a resistive ladder network **302** provides numerous different voltages to an analog multiplexer (MUX) **304** via analog signal lines **310**. One of these numerous different voltages is selected, according to the digital values on counter outputs **312**, by MUX **304** and outputs a dynamically controlled reference voltage, VREF. Resistive ladder **302** may divide down the supply voltages or another reference voltage supplied to it to generate these different voltages.

[0015] Differential receiver **308** has two inputs, REF and PAD. The PAD input is connected to the input signal being received. The REF input is connected to the dynamically controlled reference voltage, VREF. If the voltage on REF is greater than PAD, then differential receiver **308** drives signal OUT to a logical " I ". If the voltage on REF is less than PAD, then differential receiver **308** drives signal OUT to a logical "0".

[0016] Signal OUT also controls the direction of saturating binary counter **306**. By saturating binary counter it is meant that the counter outputs **312** of counter **306** does not "rollover" from its lowest value to is highest value when counting down and

does not "rollover" from its highest value to its lowest value when counting up. Instead, the counter outputs **312** reach these values and hold them until the direction control (UP/DOWN) changes state.

[0017] Counter **306** is clocked by a clock signal CK. CK typically runs at a rate that is much faster than each bit-time so that during the course of one bit-time, counter **306** could count from its lowest output value to its highest output value and visa-versa.

[0018] To illustrate the operation of the circuit shown in FIG. 3, assume that the PAD signal is at a lower voltage than the lowest analog voltage generated by resistive ladder **302** which is being output by MUX **304** as VREF and that it has been that way long enough for OUT to have commanded counter **306** to count down for enough time that counter outputs **312** have saturated at their lowest value. This is a static state as long as the voltage on PAD does not exceed VREF.

[0019] Now assume that the voltage on PAD changes from a low voltage level to a high voltage level similar to one of the changes shown in FIG. 1. This change causes PAD input to differential receiver to be higher than VREF so that differential receiver **308** changes the state of its output causing counter **306** to begin counting up with each cycle of CLK. As counter **306** counts up, counter outputs **312** cause MUX **304** to successively select increasing analog voltages generated by resistive ladder **302** with each cycle of CLK and place these successively increasing analog voltages on VREF. This results in a movement of the dynamically controlled reference voltage, VREF, moving towards a voltage level of the received voltage level on PAD. This process continues until counter outputs **312** saturate at their highest value. At this time, MUX **304** is selecting the highest analog voltage generated by resistive ladder **302** and VREF stabilizes at this voltage level until PAD changes to a voltage level lower than

VREF. This process is reversed with counter outputs **312** counting down and VREF successively decreasing when PAD changes from a high voltage level to a low voltage level similar to one of the changes shown in FIG. 1.

[0020] As shown in FIG. 1, it would be typical for the highest voltage generated by resistive ladder **302** to be less than the expected long-term steady state high voltage on PAD. Likewise, it would be typical for the lowest voltage generated by resistive ladder **302** to be more than the expected long-term steady state low voltage on PAD. Finally, it would also be typical for CLK to be about 2N times faster than the fastest cycle time of the signal on PAD, there N is the number of inputs to MUX **304**. This results in a typical transition time for VREF of about 1/2 a bit-time of the input signal on PAD. Note that almost any combination of CLK frequency and number of inputs, N, could be chosen. Values even as large or larger than 1.5 times a bit time or as small or smaller than .25 a bit time may be desirable depending upon the characteristics of the input signal.

[0021] Although a specific embodiment of the invention has been described and illustrated, the invention is not to be limited to the specific forms or arrangements of parts so described and illustrated. The invention is limited only by the claims.